ATA Host Adapter Standards Proposal

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Some technologies and techniques, which are covered in this document, are the subject of one or more patent applications.

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Revision Control

This is the first revision of this proposal.

1 – Definitions, Abbreviations, and Conventions

1.1 Definitions and Abbreviations

ADMA Command Chaining

The principle objective of implementing command chaining in the ADMA hardware is to allow the software driver and the ADMA hardware to be *loosely* coupled. To do this, the software can build up a list of tasks (a command chain) for the hardware to execute. The hardware *independently* reads these requests from memory and executes the tasks. When the hardware completes a task, it interrupts the Host to inform the Host that the task is complete, but immediately proceeds to the next task *without waiting*.

ATA Adapter

The hardware is the interface between the ATA Host and the ATA Channel. The embodiment of this hardware can be an IC or plug-in adapter.

ATA Bus

The physical connection between an ATA Adapter and an ATA Device.

ATA Channel

The ATA Channel is the logical transport mechanism between the ATA Host and the ATA Devices on an ATA Bus. Each ATA Channel can have two ATA Devices connected to it.

ATA Sub-Channel

A sub-channel controller can replace an ATA Device. A sub-channel controller can host further ATA Channels allowing extra Devices to be addressed.

ATA Device

{ATA Spec} A data storage peripheral. Traditionally, a Device on the ATA interface has been a hard drive, but any form of storage Device may be placed on the interface, provided that the Device adheres to the ATA standard.

ATA Host

The Host system in which the software that controls the functions of the ATA Subsystem is executed.

ATA Subsystem

The ATA hardware elements that includes an ATA Adapter, an ATA Channel, and ATA Device(s).

ATA-n

A shorthand reference to the standard specified in the ATA-n (or ATA/ATAPI-n, as applicable) standards document, whether published as final, circulated in draft form, or only in the planning stage.

ATA Standard

The current, evolving ATA/ATAPI standard. The standard specified by the draft of the ATA/ATAPI interface specification, NCITS document T13 1321D Revision xx, current at the time of the writing of this document.

ATA Specification

The draft of the ATA/ATAPI interface specification, NCITS document T13 1321D Revision xx current at the time of the writing of this document.

ATAPI (AT Attachment Packet Interface) Device

An ATA Device, which implements the Packet Command feature, set.

ATA Bus Release

{ATA Spec} The act of clearing both DRQ and BSY to zero before the action requested by the command is completed, to allow the Host to select the other Device on the channel. (Applies only to ATA Devices that implement Overlap Protocol, by releasing the bus.)

ATA command acceptance

{ATA Spec} A command is considered accepted whenever the currently selected Device has its Status Register Busy Bit equal to zero and the Host writes to the Device Command Register. An exception exists for following commands: Execute Device Diagnostic and Device Reset.

ATA command queue (in the Device)

{ATA Spec} The set of all commands, which the Device has accepted but whose processing the Device has not, yet completed. Command queuing allows the Host to issue concurrent commands to the same Device. Only commands in the Overlapped Feature Set may be queued.

ATA Logical Block Address (LBA)

{ATA Spec} A mode of addressing an ATA Device according to a linear mapping of sectors.

ATA Overlap Protocol

{ATA Spec} A protocol that allows ATA Devices that requires extended command execution time to perform an ATA Bus Release, so that commands may be executed by another Device on the same bus.

ATA Overlapped Command

{ATA Spec} A command is an Overlapped Command if it is included in the ATA Overlapped Feature set as defined in the {ATA Spec}.

bus protocol

The sequence of bus signal states, and their timings, which are required in order to transfer commands and data along a bus. There may be more than one protocol available on any one bus.

Cyclic Redundancy Check (CRC)

{ATA Spec} Used for the Ultra DMA protocol to check the validity of the data that has been transferred during the last Ultra DMA burst.

Direct Memory Access (DMA)

{ATA Spec} A means of data transfer, between Device and Host memory, such that Host processor intervention is not needed to accomplish the data transfer after initiation of the transfer activity.

Host DMA

For the Host, DMA Mode means that data is transferred between the Host and the ATA Adapter over the PCI bus, using the PCI Burst Mode protocol with the Adapter as master and the PCI Host as target. Once initiated, the transfer requires no Host Processor involvement.

ATA DMA

For the ATA bus, DMA means that data is transferred between the ATA Device and the ATA Adapter by a sequence of signals on the ATA bus. The ATA Adapter controls the sequence but the DMA sequence is different from that used by ATA PIO. There are two methods of DMA defined: Multiword DMA, where the Adapter, and Ultra DMA, where the sender controls the timing, controls the timings.

ATA Multiword DMA

ATA Multiword DMA is defined to transfer data at up to 16 MB/s. This protocol has traditionally been used in conjunction with the PCI DMA protocol to provide a more efficient means of transferring data through the system.

ATA Ultra-DMA

ATA Ultra-DMA is a high-speed mode of data transfer. ATA-5 defines transfer rates up to 66 MB/s, with ATA-6 slated to include a 100 MB/s rate. 32-bit ATA could increase this rate to 200 MB/s. In addition to high performance, the Ultra protocol defines the use of a CRC to validate that data has been correctly transferred.

Input/Output Manager (IOM)

The Input/Output Manager is that module in the Operating System software, which oversees the issuance of input and output commands to peripheral hardware devices.

Interrupt Request Parameter Block (IRP)

An application makes a request for data from the I/O Manager (IOM). The IOM then builds the request into an I/O Request Parameter block (IRP), and the IRP is passed by the IOM to various elements required to service the request. The request is passed to the File System, whose function is to determine where the data is located and add additional information request to the IRP

Programmed Input/Output (PIO)

{ATA Spec} A means of accessing Device registers. The term 'PIO' is also used to describe one mode of data transfer. The Host processor performs PIO data transfers, utilizing PIO accesses to the Data Register.

Host PIO

For the Host, PIO Mode means that data is transferred between the Host and the ATA Device registers, via the ATA Adapter and bus, by execution of Host-processor IN and OUT instructions with the PCI Host as master and the ATA adapter as target. This transfer method is referred to as Legacy PIO.

ATA PIO

For the ATA bus, PIO Mode means that data is transferred between the Device Adapter by the Adapter reading or writing a register in the Device. The address of the register and the timing of the transfers are under the control of the Adapter.

Ultra DMA Burst

{ATA Spec} The period from an assertion of DMACK- to the subsequent negation of DMACK-, when the Host has enabled Ultra DMA.

1.2 Conventions

Keywords

- may

A keyword indicating flexibility of choice with no implied preference.

- shall

A keyword indicating a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products conforming to this specification.

- should

A keyword indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase “it is recommended”.

Precedence.

If there is a conflict among text, figures, and tables, the precedence shall be: tables, then figures, and then text.

Names of Registers, Words, Bytes, Bits, etc.

The names of registers, words, bytes, bits, and modes begin with uppercase letters.

In addition, register names are prefixed with the acronyms PCI, ADMA, or ATA, to indicate which of these register sets they belong to.

For example: ATA Status Register, Status Word, Bytes 0-3, Error Bit.

Signal Names

Signal Names: Root Functional Name

Signal functional names are shown in all uppercase letters. For example, 'CLKRUN'

Signal Names: 'Active Low' Indicated by Suffix Letter -- 'n'

All signals are either active-high or active-low signals. If a lowercase "n” is affixed to the end of a signal name, it indicates that the signal is an active-low signal; otherwise, the signal is active-high. An active-low signal is true when the signal is below V_{IL}, and it is false when the signal is above V_{IH}. An active-high signal is true when the signal is above V_{IH}, and it is false when the signal is below V_{IL}.

For example, 'CLKRUNn' is an active-low signal.'

Signal Names: Signal-Group Prefix Letter

PCI signal names start with ‘p’. For example, 'pCLKRUNn'

ATA Channel X signal names start with ‘x’

ATA Channel Y signal names start with ‘y’

ExtATA signal names start with ‘xh’ or ‘yh’

Memory interface signal names start with ‘m’

Signal Names: Directionality Code Letter

Signal directionality codes are assigned as follows:

I = input

O = output

T = output with tristate control

B = bidirectional

C = clock input

Signal States

A signal is 'asserted' when it is driven by an active circuit to the true state. A signal is 'de-asserted' when an active circuit drives it to the false state. A signal is 'released' when it is not actively driven to any state. Some signals have bias circuitry that pulls the signal to either a true state or a false state when no signal driver is actively asserting or de-asserting the signal.

Numbers

Numbers are decimal, unless specified otherwise.

Hexadecimal numbers are shown as a string of digits, 0 through 9 or A through F, followed by 'h': e.g., '1AB7h.'

Binary numbers are shown as a string of digits, 0 or 1, followed by 'b': e.g., '10110111b'.'

2 Normative References

In addition to the references below, see also **Error! Reference source not found.**: Definitions, Abbreviations, and Conventions.

2.1 Content Imported from Normative Specifications

Where material within this specification has been imported from another, normative specification, in whole or in part, it is done so for the sake of readability of this document and the normative source document is identified. The source specification has precedence where there is a difference of definition. The references are listed in this section. Each reference has an abbreviated reference form, enclosed within braces, '{}'. This abbreviation, braces included, is used in the body of this document. Where the reference cites a standard and working drafts, the cross-reference is to the version of the reference, which was current at the time when this document was written.

2.2 Industry Standard References

2.2.1 ANSI Information Technology -- AT Attachment with Packet Interface (ATA/ATAPI)

Abbreviation: {ATA Spec}

Published standard: AT Attachment Interface with Packet Interface Extensions - 4 (ATA/ATAPI-4), ANSI National Standard for Information Systems, # X3.317-1998

Draft standard: AT Attachment Interface with Packet Interface Extensions - 5 (ATA/ATAPI-5), Proposed Draft # T13-1321D Revision 1, ANSI National Standard for Information Systems, # X3.317-1998

2.2.2 PCI Local Bus Specification

Abbreviation: {PCI Spec}

Standard for the PCI Local Bus, Revision 2.2, published December 18, 1998, by the PCI Special Interest Group (PCI SIG)

2.2.3 PCI IDE Specification

Abbreviation: {PCI IDE}

Standard for the PCI Local Bus IDE Controller, – Revision 1.0, published 4 March 1994, by the PCI Special Interest Group (PCI SIG)

2.2.4 PCI Programming Interface for IDE Bus Master Controller

Abbreviation: {PCI IDE-Programming}

Standard for the PCI Local Bus, – Revision 1.0, published 16 May 1994, by the PCI Special Interest Group (PCI SIG)

3 ATA Host Adapters

The ATA interface as defined in ATA-5 describes the physical, electrical, timing, protocol and command standards required to transfer data to and from a compliant device. That standard makes certain requirements on the Host Adapter but does not define any standards for the Host. This document defines the register and physical requirements of Host Adapters. The objective is to enable Host software device drivers to be developed that can work with a Host Adapter supplied from a variety of vendors.

Host Adapters act as a bridge between the Host computers data bus and the ATA bus. Thus Host Adapters are required to meet at least two sets of standards. Host software device drivers have to be able to configure the Adapter for both the Host bus operation and the ATA bus operation. Thus this document defines, where possible, a common API (Applications Programming Interface) for those functions.

3.1 Adapter Types

The ATA interface has evolved from an original combination of a plug in Host Adapter on the IBM PC-AT. This Adapter controlled hard drives that interfaced to it using an ST506 interface. ATA drives moved the functionality of that Adapter from a plug in card into the drive. The same register set was retained and thus the most important attribute of the ATA interface was initiated, backward compatibility. Software drivers and BIOS code did not have to change.

The first ATA Host Adapters were address decoder cards plugged into the ISA bus. The cards decoded the I/O addresses of the registers in the ATA register set and connected the ISA bus to the ATA bus. All timings on the ATA bus were those of the ISA bus. As time has progressed the performance of the ATA devices have far exceeded the capabilities of the ISA bus. The majority of Host Adapters now reside on the PCI bus and the Host Adapters have become more complex involving timing and protocol conversions as a very minimum. An ATA Host Adapter can be engineered to work on just about any bus. This document is limited to the original ISA bus and the PCI bus.

3.2 Adapter Modes

3.2.1 Legacy Mode

An Adapter is in Legacy Mode when the control of the transfer is through the ATA Command and Control Block Registers. Any data transfers are via PIO mode through the Data register. The addresses of the Command or Control block are configurable in this mode.

3.2.2 Compatibility Mode

This mode is only applicable to implementations on PC systems implementing the PC architecture. An Adapter is in Compatibility when the control of the transfer is through the ATA Command and Control Block Registers and registers in the Adapter. The addresses of the Command or Control block are defined as well as the interrupt lines (IRQs). Table 1defines the four standard I/O address banks.

Channel	Command Block Registers	Control Block Register	IRQ	Alternate IRQ
Primary	IF0h-1F7h	3F6h*	14	None
Secondary	170h-177h	376h*	15	None
Tertiary	1E8h-1EFh	3EEh	11	12 or 9
Quaternary	168h-16Fh	36Eh	10	12 or 9

Table 1-Compatibility Mode Standard I/O Register Addresses

*Note to Table 1: The Control Block registers were originally defined to include a second register at 3F7h and 377h. This register address was shared with the Floppy Disk adapter on the AT architecture. The floppy adapter uses bit 7 of that register; the hard drive adapter used bits 0-6. This register is no longer used in the ATA specification.

3.2.3 PCI Native Mode

This mode is only applicable to Adapters bridging to the PCI bus. In this mode the control of the transfer is through the ATA Command and Control Block Registers and registers in the Adapter. The addresses of the Command or Control block are defined in the BAR of the Adapter and are defined by the Host software. There is only one Host interrupt line for all the channels attached to an Adapter.

3.2.4 ADMA Mode

In this mode the ATA Command and Control Block registers are not accessible to the Host. Control is exercised through a data structure held in memory and Adapter registers.

4 ISA Address Decoder Adapter

This type of Adapter is commonly called a paddle card for use in PC compatible systems. The function of the adapter is to decode the I/O addresses appropriate to the channels it controls.

4.1 Mode of Operation

4.2 Compatibility. Detection

There is no standard method to detect the presence of this type of Adapter. Software may be able to detect the presence of ATA drives by examining the ATA registers at the standard I/O addresses and thereby infer the presence of an Adapter.

4.3 Adapter Set Up

There is no standard method used to set up these Adapters. In most cases the I/O address banks are set by hard jumpers or by vendor specific registers.

4.4 ATA Bus Timings

ISA timings. No programmable timing is available.

4.5 Electrical and Physical

The electrical and physical specifications of the ATA bus are defined in the {ATA Spec}; the ISA bus characteristics are defined in the {ISA Spec}.

4.6 Registers

The compatibility register set shall be implemented.

4.7 Operation

Only PIO transfer modes are possible.

5 PCI Compatibility and Native Mode Bus Master Adapters

PCI Adapters conforming to this standard may operate in Compatibility or Native Mode. Some adapters can be configured to operate in either mode; some are fixed to one of the modes. The mode configuration may be determined from the PCI Configuration registers.

5.1 Mode of Operation

5.1.1 Compatibility Mode

Adapters operating in compatibility mode support two channels conforming to the Primary and Secondary channel address and IRQ requirements.

5.1.2 PCI Native Mode

Adapters operating in compatibility mode may support one or two channels.

5.2 Detection

The Class Code fields determine the capabilities.

5.3 Adapter Set Up

The Class Code fields determine the capabilities of an Adapter and may be used to configure the channels to Compatibility or Native mode. The PCI BARs may be used to configure and determine the I/O addresses to use to access the ATA and Adapter registers.

5.4 ATA Bus Timings

Determination of the ATA PIO timings, DMA protocols and DMA timings supported is vendor specific. Consequently configuring these attributes is vendor specific.

5.5 Electrical and Physical

The electrical and physical specifications of the ATA bus are defined in the {ATA Spec}; the PCI bus characteristics are defined in the PCI2.2 specification.

5.6 PCI Registers

The PCI Adapter implements a subset of the PCI standard type 00h configuration header register set. All registers have the standard meaning as defined in the PCI Specification, Issue 2.2. The registers with specific meanings with respect to this standard are defined below. Register contents that are otherwise defined in the PCI standard are indicates as “PCI”. Fields marked 'reserved' are all zeros and read only.

Byte Offset	Bits 31-24	Bits 23-16	Bits 15-8	Bits 7-0
00h	PCI		PCI	
04h	PCI		PCI	
08h	Class Code			PCI
0Ch	PCI	PCI	PCI	PCI
10h	Base Address 0 -- Base Address of Cmd-Block Regs, ATA Channel X			
14h	Base Address 1 -- Base Address of Control Regs, ATA Channel X			
18h	Base Address 2 -- Base Address of Cmd-Block Regs, ATA Channel Y			
1Ch	Base Address 3 -- Base Address of Control Regs, ATA Channel Y			
20h	Base Address 4 -- Base Address of ATA Bus Master Registers			
24h	Reserved			
28h	PCI			
2Ch	Subsystem ID		PCI	
30h	PCI			
34h	PCI			PCI
38h	PCI			
3Ch	PCI	PCI	PCI	Interrupt Line

5.6.1 PCI Class Code

The class code indicates that the Adapter is a mass storage controller (Base Class = 01), ATA controller (Sub-Class = 01), Native or Compatibility Mode Depending on the value in the Programming Interface Byte.

Address Offset 09h
Default Value 01010xh
Attribute Base and Sub-Class Bytes are Read Only. The attribute of the Programming Interface Byte is implementation dependant.
Size 24 bits

5.6.1.1 Programming Interface Byte

Table 2 defines the usage and values of the Programming and Interface Byte.

Bit	Description
0	Determines the mode that the primary ATA channel is operating in. Clearing this bit to zero corresponds to 'compatibility', setting the bit to one means native-PCI mode. This bit is implemented as read-only if the channel supports only one mode, or read-write if both modes are supported. For implementations that support both modes the power on and hardware reset states are vendor specific.
1	This bit indicates whether or not the primary channel has a fixed mode of operation. If this bit is cleared to zero, the mode is fixed and is determined by the (read-only) value of bit 0. If this bit is set to one, the channel supports both modes and may be set to either mode by writing bit 0.
2	Determines the mode that the secondary ATA channel is operating in. Clearing this bit to zero corresponds to 'compatibility', setting the bit to one means native-PCI mode. This bit is implemented as read-only if the channel supports only one mode, or read-write if both modes are supported. For implementations that support both modes the power on and hardware reset states are vendor specific.
3	This bit indicates whether or not the secondary channel has a fixed mode of operation. If this bit is cleared to zero, the mode is fixed and is determined by the (read-only) value of bit 0. If this bit is set to one, the channel supports both modes and may be set to either mode by writing bit 0.

Table 2: PCI Adapter bit definitions in Programming Interface byte

5.6.2 PCI Base Address Registers (BAR)

Base Address Registers 0-3 have Bit 0 hard-wired to 1 to indicate I/O space.

5.6.2.1 PCI Base Address 0

This is the base address for the command block registers for ATA Channel X.
Address Offset 10h
Default Value 000001F1h

When operating in compatibility mode any write to the BAR shall be ignored and the default value shall always be used. In compatibility mode an independent IRQ shall be provided that is connected to IRQ14. When the Adapter is disabled (using the IO Enable bit in the PCI Command register), the Adapter shall not respond to any IO addresses, and shall tri-state its IRQ connections.
Attribute Bits 31-16 may be Read Only, Bits 15-3 Read/Write, Bits 2-0 Read Only
Size 32 bits

5.6.2.2 PCI Base Address 1

This is the base address for the control register for ATA Channel X. Note that, because of the Dword alignment of PCI, the Device Control and Alternate Status Registers are at offset 02h from this base. For example, to put those registers at address 3F6h, this register shall be set to 3F4h (+ Bit 0).
Address Offset 14h
Default Value 000003F5h
When operating in compatibility mode any write to the BAR shall be ignored and the default value shall always be used.
Attribute Bits 31-16 may be Read Only, Bits 15-3 Read/Write, Bits 2-0 Read Only.
Size 32 bits

5.6.2.3 PCI Base Address 2

This is the base address for the command block registers for ATA Channel Y

Address Offset 18h

Default Value 00000171h

When operating in compatibility mode any write to the BAR shall be ignored and the default value shall always be used. In compatibility mode an independent IRQ shall be provided that is connected to IRQ15. When the Adapter is disabled (using the IO Enable bit in the PCI Command register), the Adapter shall not respond to any IO addresses, and shall tri-state its IRQ connections

Attribute Bits 31-16 may be Read Only; Bits15-3 Read/Write; Bits 2-0 Read Only.

Size 32 bits

5.6.2.4 PCI Base Address 3

If the device implements two channels this is the base address for the control registers for ATA Channel Y.

Address Offset 1Ch

Default Value 00000375h

When operating in compatibility mode any write to the BAR shall be ignored and the default value shall always be used.

Attribute Bits 31-16 may be Read Only, Bits 15-3 Read/Write, Bits 2-0 Read Only.

Size 32 bits

5.6.2.5 PCI Base Address 4

Base address of the ATA Bus Master I/O registers.

Address Offset 20h

Default Value 00000000h

Attribute Bits 31-16 may be Read Only, Bits 15-3 Read/Write, Bits 2-0 Read Only.

Size 32 bits

5.6.3 PCI Interrupt Line

The Host BIOS and O/S Drivers may use this location to store the system interrupt (IRQ) allocated to this device. The Adapter does not use this information. BIOS and O/S Drivers may use this location to store the information. When the Adapter is in compatibility mode the value in this register has no meaning since the IRQs are predetermined for each channel.

Address Offset 3Ch

Default Value 00h

5.7 ATA Bus Master Registers

The bus master IDE function uses 16 bytes of IO space. All bus master IDE IO space registers can be accessed as byte, word, or Dword quantities. The description of the 16 bytes of IO registers follows:

Offset from Base Address	Register	Register Access
00h	ATA Bus Master Command register Primary	R/W
01h	Device Specific	
02h	ATA Bus Master Status register Primary	RWC
03h	Device Specific	
04h-07h	ATA Bus Master PRD Table Address Primary	R/W
08h	ATA Bus Master Command register Secondary	R/W
09h	Device Specific	
0Ah	ATA Bus Master Status register Secondary	RWC
0Bh	Device Specific	
0Ch-0Fh	ATA Bus Master PRD Table Address Secondary	R/W

Table 3 ATA Bus Master Register Offsets

5.7.1 ATA Bus Master Command Register

Register Name: ATA Bus Master Command Register

Address Offset: Primary Channel: Base + 00h

Secondary Channel: Base + 08h

Default Value: 00h

Attribute: Read / Write

Size: 8 bits

Bit	Description
7:4	**Reserved.** Must return 0 on reads.
3	**Read or Write Control:** This bit sets the direction of the bus master transfer: when cleared to zero, PCI bus master reads are performed. When set to one, PCI bus master writes are performed. This bit shall NOT be changed when the bus master function is active.
2:1	**Reserved. Shall** return 0 on reads.
0	**Start/Stop Bus Master:** Bus master operation of the Adapter is enabled by setting this bit to one. Bus master operation begins when this bit is detected changing from a zero to a one. The Adapter shall only transfer data between the ATA device and memory only when this bit is set to one. Master operation may be halted by clearing this bit to zero. All state information is lost when a '0' is written; Master mode operation cannot be stopped and then resumed. If this bit is reset while bus master operation is still active the bus master command is aborted and data transferred from the drive may be discarded before being written to system memory. This bit is intended to be reset after the data transfer is completed, as indicated by either the Bus Master ATA Active bit or the Interrupt bit of the Bus Master ATA Status register for that ATA channel being set to one, or both.

Table 4 ATA Bus Master Command Register

5.7.2 ATA Bus Master Status Register

Register Name: Bus Master ATA Status Register

Address Offset: Primary Channel: Base + 02h

Secondary Channel: Base + 0Ah

Default Value: 00h

Attribute: Read/Write Clear

Size: 8 bits

Bit	Description
7	**Simplex only:** This read-only bit indicates whether or not both bus master channels (primary and secondary) can be operated at the same time. If the bit is a '0', then the channels operate independently and can be used at the same time. If the bit is a '1', then only one channel may be used at a time.
6	**Drive 1 DMA Capable:** This read/write bit is set by device dependent code (BIOS or device driver) to indicate that drive 1 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance.
5	**Drive 0 DMA Capable:** This read/write bit is set by device dependent code (BIOS or device driver) to indicate that drive 0 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance.
4:3	**Reserved.** Must return 0 on reads.
2	**Interrupt:** This bit is set to one by the rising edge of the ATA channel's interrupt line. This bit is cleared to zero when a '1' is written to it by software. Software can use this bit to determine if an ATA device has asserted its interrupt line. When this bit is read as a one, all data may have been transferred from the Device to the Host's system memory. The Adapter shall not set this bit to one until it has flushed any internal data buffers.
1	**Error:** This bit is set when the controller encounters an error in transferring data to/from memory. The exact error condition is bus specific and can be determined in a bus specific manner. This bit is cleared when a '1' is written to it by software.
0	**Bus Master IDE Active:** This bit is set to one when the Start bit is written to the ATA Bus Master Command registers. This bit is cleared to zero when the last transfer for a region is performed, where EOT for that region is set in the region descriptor. It is also cleared when the Start bit is cleared in the ATA Bus Master Command register. When this bit is read as a zero, all data transferred from the drive during the previous bus master command has been transferred to the Host's system memory, unless the bus master command was aborted.

Table 5 Bus Master ATA Status Register

5.7.3 PRD Table Pointer Register

Register Name: Descriptor Table Pointer Register

Address Offset: Primary Channel: Base + 04h

Secondary Channel: Base + 0Ch

Default Value: 00000000h

Attribute: Read / Write

Size: 32 bits

Bit	Description
31:2	Base address of Descriptor table. Corresponds to A[31:2]
1:0	Reserved

Table 6 PRD Table Pointer Register

The PRD Table must be Dword aligned. The Descriptor Table must not cross a 64K boundary in memory.

5.8 Interrupt Line Considerations

When a channel is in compatibility mode the IRQ used by the channel shall be the compatibility' IRQ. PCI interrupt lines shall not be affected by that channel's interrupt. Conversely, when the channel is in native-PCI mode the channel's interrupt shall be connected to the appropriate INTx#. Compatibility IRQs shall not be affected and if connected shall be tri-stated.

Connections of channel interrupt signals to the compatibility IRQs shall be tri-stated until the Adapter is enabled via the PCI Command register in PCI Configuration Space. The Adapter is enabled when a '1' is written to the IO enable bit (bit 0) in the Command register.

5.9 Bus Master Operation

When transferring data to or from an ATA device using an ATA DMA protocol the Adapter uses PCI Bus Master protocols to transfers the data to or from the Host's memory.

The master mode-programming interface is an extension of the standard ATA programming model. This means that devices can always be dealt with using the standard ATA programming model, with the master mode functionality used when the appropriate driver and devices are present. Master operation is designed to work with any ATA device that supports DMA transfers on the ATA bus. Devices that only work in PIO mode can be used through the standard ATA programming model.

The programming interface defines a simple scatter/gather mechanism allowing large transfer blocks to be scattered to or gathered from memory. This cuts down on the number of interrupts to and interactions with the CPU.

Master ATA Adapters shall default to Mode 0 Multiword DMA timings to ensure operation with DMA capable ATA devices without the need for Adapter vendor-specific code to initialize Adapter-specific timing parameters.

5.9.1 Physical Region Descriptor Table

Before the Adapter starts a master transfer it is given a pointer to a Physical Region Descriptor Table (PRD Table). This table contains some number of Physical Region Descriptors (PRDs), which describe areas of memory that are involved in the data transfer. The descriptor table must be aligned on a 4-byte boundary and the table cannot cross a 64K boundary in memory.

5.9.2 Physical Region Descriptor

The physical memory region to be transferred is described by a Physical Region Descriptor (PRD). The data transfer will proceed until all regions described by the Prods in the table have been transferred.

Each PRD entry is 8 bytes in length. The first 4 bytes specify the byte address of a physical memory region. The next two bytes specify the count of the region in bytes (64K byte limit per region). A value of zero in these two bytes indicates 64K. Bit 7 of the last byte indicates the end of the table; bus master operation terminates when the last descriptor has been retired.

<table>
<tr><td></td><td colspan="2">Byte 3</td><td colspan="2">Byte 2</td><td>Byte 1</td><td>Byte 0</td></tr>
<tr><td>Dword 0</td><td colspan="5">Memory Region Physical Base Address [32:1]</td><td>0</td></tr>
<tr><td>Dword 1</td><td>EOT</td><td colspan="3">Reserved</td><td>Byte Count [15:1]</td><td>0</td></tr>
</table>

Figure 1 Physical Region Descriptor Table Entry

The memory region specified by the descriptor is further restricted such that the region cannot straddle a 64K boundary. The sum of the descriptor byte counts must be equal to, or greater than the size of the disk transfer request. If greater than, then the driver must terminate the Bus Master transaction (by resetting bit zero of the ATA Bus Master Command register to zero) when the drive issues an interrupt to signal transfer completion.

5.9.3 Standard Programming Sequence

To initiate a bus master transfer between memory and an ATA DMA device, the following steps are required:

1. Software prepares a PRD Table in system memory. Each PRD is 8 bytes long and consists of an address pointer to the starting address and the transfer count of the memory buffer to be transferred. In any given PRD Table, two consecutive Prods are offset by 8-bytes and are aligned on a 4-byte boundary.
2. Software provides the starting address of the PRD Table by loading the PRD Table Pointer Register. Setting of the Read/Write Control bit specifies the direction of the data transfer. Clearing the Interrupt and Error bits in the ATA Bus Master Status register to zero readies the Adapter for a data transfer.
3. Engage the bus master function by writing a '1' to the Start bit in the ATA Bus Master Command Register for the appropriate channel.
4. Software issues the appropriate DMA transfer command to the disk device.
5. The controller transfers data to/from memory responding to DMA requests from the ATA device.
6. At the end of the transfer the ATA device signals an interrupt.
7. For transfers from the Device to the Host the Adapter shall first flush any internal data buffers before asserting the Host interrupt signal.

8. In response to the interrupt, software resets the Start/Stop bit in the ATA Bus Master Command register. The software then reads the Adapter status and then the Device status to determine if the transfer completed successfully.

5.9.4 ATA Bus Master Status Register Bit Interpretation

The table below gives a description of how to interpret the Interrupt and Active bits in the Controller status register after a DMA transfer has been started.

Interrupt	Active	Description:
0	1	DMA transfer is in progress and the ATA device has not asserted an interrupt.
1	0	The ATA device asserted the interrupt signal and the Adapter exhausted the Prods. This is the normal completion case where the size of the physical memory regions was equal to the ATA device transfer size.
1	1	The ATA device asserted the interrupt signal but the Adapter has not reached the end of the physical memory regions. This is a valid completion case where the size of the physical memory regions was larger than the ATA device transfer size.
0	0	This bit combination signals an error condition. If the Error bit in the ATA Bus Master Status register is set to one, then the Adapter has some problem transferring data to/from memory. Specifics of the error have to be determined using bus-specific information. If the Error bit is not set, then the Prod's specified a smaller size than the ATA transfer size.

Table 7 ATA Bus Master Status Register Bits

5.9.5 Error Conditions

If the controller encounters an error while doing the bus master transfers it will stop the transfer (i.e. reset the Active bit in the ATA Bus Master Command register) and set the ERROR bit in the ATA Bus Master Status register. The controller does not generate an interrupt when this happens. The device driver may use device specific information (e.g.; PCI Configuration Space Status register) to determine what caused the error.

6 ADMA Mode Adapters

6.1 Background

The performance of ATA Devices has increased dramatically over the last few years, including the introduction of the Overlapped and Queued Command set. However, systems using these faster Devices have not shown all of the expected benefits. This limited performance improvement can be traced to the design and implementation of the ATA Host adapters currently in use.

The objective of the ADMA design is to drastically increase the performance of systems that use ATA Devices. To fully optimize the system throughput, it implements a command chaining technique to de-couple the Host command sequence from the channel execution. This allows true multitasking and the ability to effectively exploit the Overlapped and Queued Command set as defined in the {ATA Spec}.

6.2 Operating Modes

Two modes of operation are implemented, Legacy mode (power-on default) and Automatic DMA mode.

6.2.1 Legacy Mode

The basic operation of any ATA subsystem is in legacy PIO Mode. This means that the ATA Adapter acts as an address decoder for the Host. All reads and writes are performed using Host I/O instructions. The only function performed by the ATA Adapter is to control the signal timings of the ATA bus and to respond to the PCI signals. In this mode, all data transfers use the PIO protocols.

6.2.2 Automatic DMA Mode

The Adapter autonomously follows a command chain in memory as described in Section 6.8.1. In this mode, data transfers can be either Ultra DMA or DMA-assisted PIO.

6.3 Detection

The Adapter is detectable by examining the PCI Device ID, Class Code and Revision ID. These three combined will define the exact specification level to which the Adapter conforms.

6.4 Adapter Set Up

The Adapters registers are configurable through the PCI Configuration registers. The Adapter's ATA transfer modes are configurable through registers and within the data structures for ADMA mode transfers.

6.5 Electrical and Physical

The PCI bus characteristics are defined in the PCI2.2 specification. The electrical and physical specifications of the ATA bus are defined in the {ATA Spec} with the additions as noted below.

6.5.1 Electrical Characteristics

The electrical characteristics of these signals are the same as the ATA signals defined in ATA-5.

6.5.2 x/yUIRQn -- ATA Channels

Pin 20 (40 pin header) of the ATA bus. This signal is pulled high by the Adapter using a 10k ohm resistor and asserted (pull low) by either Device to indicate that an event has occurred.

6.5.3 ExtATA Signals

The ExtATA signals are used on systems implementing External ATA interface.

6.5.3.1 yhHPRES -- ExtATA

Adapter (Host) present and powered. This signal is used to activate the power supply, if any, in the external device. The signal is reflected back to the Adapter on yhDPRES when the external device is present and powered.

6.5.3.2 yhDPRES – ExtATA Device Present

Asserted by the remote Device to indicate that it is present and powered. The signal shall be pulled low at the Host, using a 10k-ohm resistor. The input shall be implemented with hysteresis (i.e. Schmitt trigger) and shall have an external time delay circuit with a time constant of at least 1ms. While this signal is de-asserted, all of the signals on the Adapter's channels shall be tri-stated (except yhHPRES and yRSTn, which shall be asserted.). This signal shall default to asserted at power-on or reset. It may be asserted or de-asserted by setting HP to one, or by clearing HP to zero in the Channel Ping Register.

6.5.3.3 yhDIRn -- ExtATA Direction

Asserted by the Adapter to indicate that the Adapter is reading data and that the external device™ may assert its drivers.

6.5.3.4 yhRTHDn -- ExtATA Reflective Timing, Host to Device

Asserted by the Adapter to determine the round-trip delay of the cable and the buffers. For ATA PIO transfers, this signal is asserted simultaneously with the assertion of yIORn or yIOWn.

This signal is also used to measure the round-trip delay of the connected circuit, using the PING Register.

6.5.3.5 yhRTDHn -- ExtATA Reflective Timing, Device to Host

Asserted by the Device, in response to yhRTHDn. For ATA PIO transfers, assertion of this signal starts the timing of the active elements of IOR or IOW.

This signal is also used to measure the round-trip delay of the connected circuit, using the sub-channel PING command.

6.6 PCI Configuration Header Registers

The Adapter implements a subset of the PCI standard type 00h configuration header register set. All registers have the standard meaning as defined in the PCI Specification, Issue 2.2. The registers with specific meanings with respect to this standard are defined below. Register addresses that are otherwise defined in the PCI standard are indicates as “PCI”. Fields marked 'reserved' are all zeros and read only.

Byte Offset	Bits 31-24	Bits 23-16	Bits 15-8	Bits 7-0
00h	PCI Device ID		PCI	
04h	PCI		PCI	
08h	Class Code			Revision
0Ch	PCI	PCI	PCI	PCI
10h	Base Address 0 -- Base Address of Cmd-Block Regs, ATA Channel X			
14h	Base Address 1 -- Base Address of Control Regs, ATA Channel X			
18h	Base Address 2 -- Base Address of Cmd-Block Regs, ATA Channel Y			
1Ch	Base Address 3 -- Base Address of Control Regs, ATA Channel Y			
20h-27h	Base Address 4 -- Base Address of Memory-Mapped ATA Channel and ADMA Registers			
28h	PCI			
2Ch	Subsystem ID		PCI	
30h	PCI			
34h	PCI			PCI
38h	PCI			
3Ch	PCI	PCI	PCI	Interrupt Line

Table 8 – PCI Configuration Space Header Registers

6.6.1 PCI Device ID

Indicates that the Device conforms to this series of specifications.

Address offset	02h
Default Value	1841h
Attribute	Read Only
Size	16 bits

6.6.2 PCI IC Revision

Indicates that it conforms to revision 4 of this specification series.

Address Offset	08h
Default Value	40h
Attribute	Read Only
Size	8 bits

4xh Indicates that this device conforms to this specification. x0h indicates that this device is the first revision of the IC. If errors are discovered that require a change to this IC the second nibble will be incremented. Any functional change to the specification will require an up issue of the spec and thus the most significant nibble.

6.6.3 PCI Class Code

The class code indicates that the Adapter is a mass storage controller (01), ATA controller (01), Bus Master Command Chain PCI Native Mode only.

Address Offset 09h
Default Value 010520h (Non-Chained Controller)
010530h (Chained Controller)
Attribute Read Only
Size 24 bits

6.6.4 PCI Base Address Registers (BAR)

Base Address Registers 0-3 have Bit 0 hard-wired to 1 to indicate I/O space and Bits 16-31 hard-wired to zero. Full address decoding shall be implemented.

6.6.4.1 PCI Base Address 0
This is the base address for the command block registers for ATA Channel X.
Address Offset 10h
Default Value 000001F1h
Attribute Bits 31-16 Read Only, Bits 15-3 Read/Write, Bits 2-0 Read Only.
Size 32 bits

6.6.4.2 PCI Base Address 1
This is the base address for the control registers for ATA Channel X. Note that, because of the Dword alignment of PCI, the Device Control and Alternate Status Registers are at offset 02h from this base. For example, to put those registers at address 3F6h, this register shall be set to 3F4h (+ Bit 0).
Address Offset 14h
Default Value 000003F5h
Attribute Bits 31-16 Read Only, Bits 15-3 Read/Write, Bits 2-0 Read Only.
Size 32 bits

6.6.4.3 PCI Base Address 2
If the device implements two channels this is the base address for the command block registers for ATA Channel Y
Address Offset 18h
Default Value 00000171h
Attribute Bits 31-16 Read Only; Bits15-3 Read/Write; Bits 2-0 Read Only.
Size 32 bits

6.6.4.3.1 PCI Base Address 3
If the device implements two channels this is the base address for the control registers for ATA Channel Y.
Address Offset 1Ch
Default Value 00000375h
Attribute Bits 31-16 Read Only, Bits 15-3 Read/Write, Bits 2-0 Read Only.
Size 32 bits

6.6.4.4 PCI Base Address 4 and 5
This is the base address for the 64 bit Memory Mapped ADMA registers.
Address Offset 20h
Default Value 0000000000000004h
Attribute Bits 31-10 Read/Write; Bits 9-0 Read Only.
Size 64 bits

6.6.5 PCI Interrupt Line

The Host BIOS and O/S Drivers may use this location to store the system interrupt (IRQ) allocated to this device. The Adapter does not use this information. When the Adapter is in compatibility mode the value in this register has no meaning since the
Address Offset 3Ch
Default Value 00h

6.7 ATA and ADMA Register Memory Map

The bus mastering function uses 1024 bytes of memory space. The ATA I/O registers are mapped into memory space. Access to the legacy registers may be via I/O or memory. All Host registers can be accessed as byte, word or Dword entities. These Registers are addressed via the base address in BAR 4 (Bytes 20h-27h) in the configuration header registers. The description of the DMA registers follows.

Offset	Bits 31-24	Bits 23-16	Bits 15-8	Bits 7-0
00h	Reserved		Chan. X PIO Data	
04h	Reserved			Chan. X Err. /Features
08h	Reserved			Chan. X Sector Cnt.
0Ch	Reserved			Chan. X Sect. Numb.
10h	Reserved			Chan. X Cyl. Low
14h	Reserved			Chan. X Cyl. High
18h	Reserved			Chan. X Dev. Head
1Ch	Reserved			Chan. X Stat/Cmd
20h-34h	Reserved			
38h	Reserved			Chan. X Alt. Stat./ Dev. Cntl.
3Ch	Reserved			
40h	Reserved		Chan. Y PIO Data	
44h	Reserved			Chan. Y Err. /Features
48h	Reserved			Chan. Y Sector Cnt.
4Ch	Reserved			Chan. Y Sect. Numb.
50h	Reserved			Chan. Y Cyl. Low
54h	Reserved			Chan. Y Cyl. High
58h	Reserved			Chan. Y Dev. Head
5Ch	Reserved			Chan. Y Stat/Cmd
60h-74h	Reserved			
78h	Reserved			Chan. Y Alt. Stat./ Dev. Cntl.
7Ch	Reserved			
80h	Reserved	Chan. X ADMA Status	Reserved	Chan. X ADMA Control
84h	Reserved		Chan. X ADMA CPB Search Count	
88h	Chan. X ADMA Current CPB Address			
8Ch	Chan. X ADMA Next CPB Address			
90h	Chan. X CPB Lookup Table Address			
94	Chan. X ADMA Output FIFO Threshold		Chan. X ADMA Input FIFO Threshold	
98-9Ch	Reserved			
A0h	Reserved	Chan. Y ADMA Status	Reserved	Chan. Y ADMA Control
A4h	Reserved		Chan. Y ADMA CPB Search Count	
A8h	Chan. Y ADMA Current CPB Address			
ACh	Chan. Y ADMA Next CPB Address			
B0h	Chan. Y CPB Lookup Table Address			
B4h	Chan. Y ADMA Output FIFO Threshold		Chan. Y ADMA Input FIFO Threshold	
B8h-BCh	Reserved			
C0h	BIOS Access Address Register			
C4h	Reserved	Ping Register	Reserved	Reserved
C8h-D0h	Reserved			
D4h	BIOS Message Pointer			
D8h	Reserved			
DCh	Driver Message Pointer			
E0h-3FFh	Reserved			

Table 9 – ATA and ADMA Memory Mapped Registers

6.7.1 ATA Legacy Registers

Address offset, Channels X and Y: Base + 00h

When operating in ADMA Mode, the ATA legacy registers are not available. Any access to the ATA Status (or ATA Alternate Status) shall return a value with Bit 7 (busy) being set. Any read to other registers shall return an indeterminate value. Any write to an ATA register shall be ignored.

6.7.2 ADMA Control Register (ADMCTL)

Address offset, Channel X: Base + 80h

Address offset, Channel Y: Base + A0h

Default value 00h

Attribute Read/Write

Size 8 bits

Bit	Name	Cntrl	Reset	Description
7	aGO	H/H	0	ADMA GO bit. When cleared to 0 and the Adapter is currently in ADMA Mode, the Adapter shall finish the current operation and revert to Legacy Mode. The Host writes a one to this bit each time a valid CPB has been assembled, to notify the Adapter that there is another CPB ready for service.
6	aPSE	H/H	0	ADMA PAUSE bit. When set to 1, the Adapter shall not follow the CPB chain nor access the CPB Lookup Table. If set to one while a CPB is being processed, the Adapter shall complete the CPB and then PAUSE. The S/W driver to pause operations before modifying the CPB chain pointers shall use aPSE. The Host can safely access the CPB chain, once the Adapter is paused.
5	aRSTADM	H/H	0	Adapter hardware reset bit. To reset the Adapter, set aRSTADM to one for at least two PCI clock cycles then clear it.
4	aSUBEN	H/H	0	ADMA SUB-CHANNEL ENABLE bit. When set to 1, the Adapter allows the use of non-zero sub- channel numbers.
3	aAUTEN	H/H	0	ADMA AUTO-POLL ENABLE bit. This bit is used in an overlapped or queued operation. When set to 1, the Adapter shall alternately poll each device on a channel. Polling involves the Adapter toggling the ATA DEV bit and the ATA interrupt line (INTRQ) is asserted, the ATA register is read and the state of SERV bit is determined and processed accordingly.
2	aRSTA	H/H	0	ATA HARD RESET bit. When set to 1, the ATA reset signal is asserted. For the Host to reset the ATA channel, the Host shall set this bit to one, wait for the minimum reset time defined in the ATA Spec and the Host shall then clear this bit to zero.
1:0	aPIOMD	H/H	00	Default PIO Mode. Used in Legacy Mode to define the ATA PIO timing. 00 = Mode 1, 01 = Mode2, 10 = Mode 3, 11 = Mode 4. The mode defined in this register is used for all accesses to the ATA command and control block registers. It is used for access to the ATA Data Register in legacy mode but is not used for access to the ATA Data Register in the DMA assisted PIO mode.

Table 10 – ADMA Control Register

6.7.3 ADMA Status Register (ADMSTAT)

Address offset, Channel X: Base + 82h

Address offset, Channel Y: Base + A2h

Default value 80h

Size 8 bits

Attribute Read/Clear

The Host may read this register at any time. Reading the register clears all the bits to zero and de-asserts pINTA.

Bit	Name	Cntrl	Reset	Description
7	aDONE	P/S	0	ADMA DONE bit. When set to 1, indicates the Adapter has finished one or more CPBs in the chain.
6	aPSD	P/C	X	ADMA PAUSED bit. When set to 1, indicates the Adapter is in Paused state (see 6.11.5.4)
5	aSTPD	P/C	1	ADMA STOPPED bit. When set to 1, indicates the Adapter is either in Legacy Mode or idled in ADMA Mode depending on the state of aLGCY. See 6.11.5 for detailed explanation of this bit
4	aUIRQ	P/P	X	ATA UNSOLICITED IRQ bit. When set to 1, indicates the ATA unsolicited interrupt line is active.
3	aLGCY		0	When set to 1, indicates the Adapter is in Legacy Mode.
2			0	Reserved.
1	aCPBERR	P/S	0	Indicates that at least one of the error bit in the CPB Response byte has been set to one (see Table 13).
0	aPERR	P/S	0	PCI ERROR bit. When set to 1, indicates that a PCI error has occurred.

Table 11 – ADMA Status Register

6.7.4 ADMA CPB Search Count Register (CCNT)

Address offset, Channel X: Base + 84h

Address offset, Channel Y: Base + A4h

Default value 0000h

Attribute Read/Write

Size 16 bits

The ADMA CPB Search Count Register holds a value that is copied into the Internal Down-Counter each time either a write occurs to the ADMA Control Register with the ADMA aGO bit set or the Adapter reads a CPB with the cVALID bit set and the cDONE bit clear. The down-counter decrements each time the Adapter reads a CPB with the cVALID bit clear, cREL set to one or the cDONE bit set to one. When the down counter reaches zero, the Adapter sets aDONE and transitions to the IDLE state. The value loaded into this register is normally (but not necessarily) related to the number of CPBs in the chain.

6.7.5 ADMA Current CPB Address (CCPB)

Address offset, Channel X: Base + 88h

Address offset, Channel Y: Base + A8h

Default value 00000000h

Attribute Read

Size 32 bits

The ADMA Current CPB Address Register points to the address of the CPB currently being processed. The Adapter loads it whenever a CPB is read, (or, in the case of queued operation, reads the CPB Lookup Table).

6.7.6 ADMA Next CPB Address (NCPB)

Address offset, Channel X: Base + 8Ch

Address offset, Channel Y: Base + ACh

Default value 00000000h

Attribute Read/Write

Size 32 bits

The ADMA Next CPB Address Register is initialized by the Host to point to the ‘first’ CPB in a circular chain, which it has constructed in memory. The address shall be a physical address***.*** This register is updated by the Adapter each time it reads a CPB, except when retrieving a CPB from the lookup table. The Host shall not write to this register while the Adapter is active (that is, not IDLE, STOPPED, nor PAUSED).

Note that each CPB shall be physically contiguous and locked in memory and that all chain pointers shall be physical addresses.

6.7.7 CPB LookUp Table Address Register

Address offset, Channel X: Base + 90h

Address offset, Channel Y: Base + B0h

Default value 00000000h

Attribute Read/Write

Size 32 bits

The CPB LookUp Table Address Register is only used in overlapped or queued operation. It is initialized by the Host to point to the base of a lookup table, which it has constructed in memory. The address shall be a ***physical address***. This register is used by the Adapter to construct the address of the applicable CPB when a service interrupt is received (in overlapped or queued operation). Each entry in the table is a Dword holding the ***physical address*** of the CPB. The address of the entry is constructed as

Lookup Table Address + (Sub-Channel * 200h) + (Device * 100h) + (Tag * 08h)

Note that the CPB LookUp Table shall be physically contiguous and locked in memory

6.7.8 Channel-Y PING Register

Address offset, Base + C6h

Default value 10X00000b

Attribute Read/Write

Size 8 bits

b0-b4	Reflective Count	The number of 10ns clock periods from the assertion of yhRTHD to the assertion of yhRTDHn. A value of zero after the setting of PING indicates that there is no delay. Shall default to 00000b. When the maximum value is reached (11111b, the counter shall stop.
b5	DPRES	Reflects the current state of yhDPRS (1 = asserted, 0 = de-asserted)
b6	PING	The Host's setting PING to one causes the reflective count to be cleared to zero and yhRTHD to be asserted. The Host's clearing PING to zero shall release yhRTHD.
b7	HPON	The Host's setting HPON to one shall assert yhHPRES. The Host's clearing HPON shall de-assert yhHPRES. HPON shall default to one.

Table 12 Ping Register

6.7.9 Message Pointer

This register is used by the BIOS to point to its message area. The Adapter takes no action on this register other than clearing it on reset. The data structure used is described in .

Address Offset D4h

Default Value 00000000h

Attribute Read/Write

Size 32 bits

6.7.10 Driver Message Pointer

This register is used by the Host driver to point to its message area. The Adapter takes no action on this register other than clearing it on reset. The data structure used is described in .

Address Offset DCh

Default Value 00000000h

Attribute Read/Write

Size 32 bits

6.8 Data Structures

. ATA/ATAPI command set/sets and their associated controls and status are held in a data structure termed Command Parameter Block (CPB). A chain of CPBs can be created in Host memory. This is a circular chain with each CPB pointing to the next CPB and the last CPB points to the first CPB to complete the chain.

Within each CPB, there is a pointer to the Physical Region Descriptor (PRD). The PRD is a data structure that defines the memory locations where the data is to be written to or read from. A chain of PRDs can be created in

Host memory to implement a memory scatter-gather list. This is a chain with each PRD pointing to the next PRD and the last PRD is indicated by a bit in the PRD entry.

All address pointers shall be physical addresses.

Each PRD or CPB entry shall be physically contiguous and quad-word aligned in host unpaged physical address space.

In Auto DMA Mode, the Adapter reads in, from Host memory, a command set held in the command chain

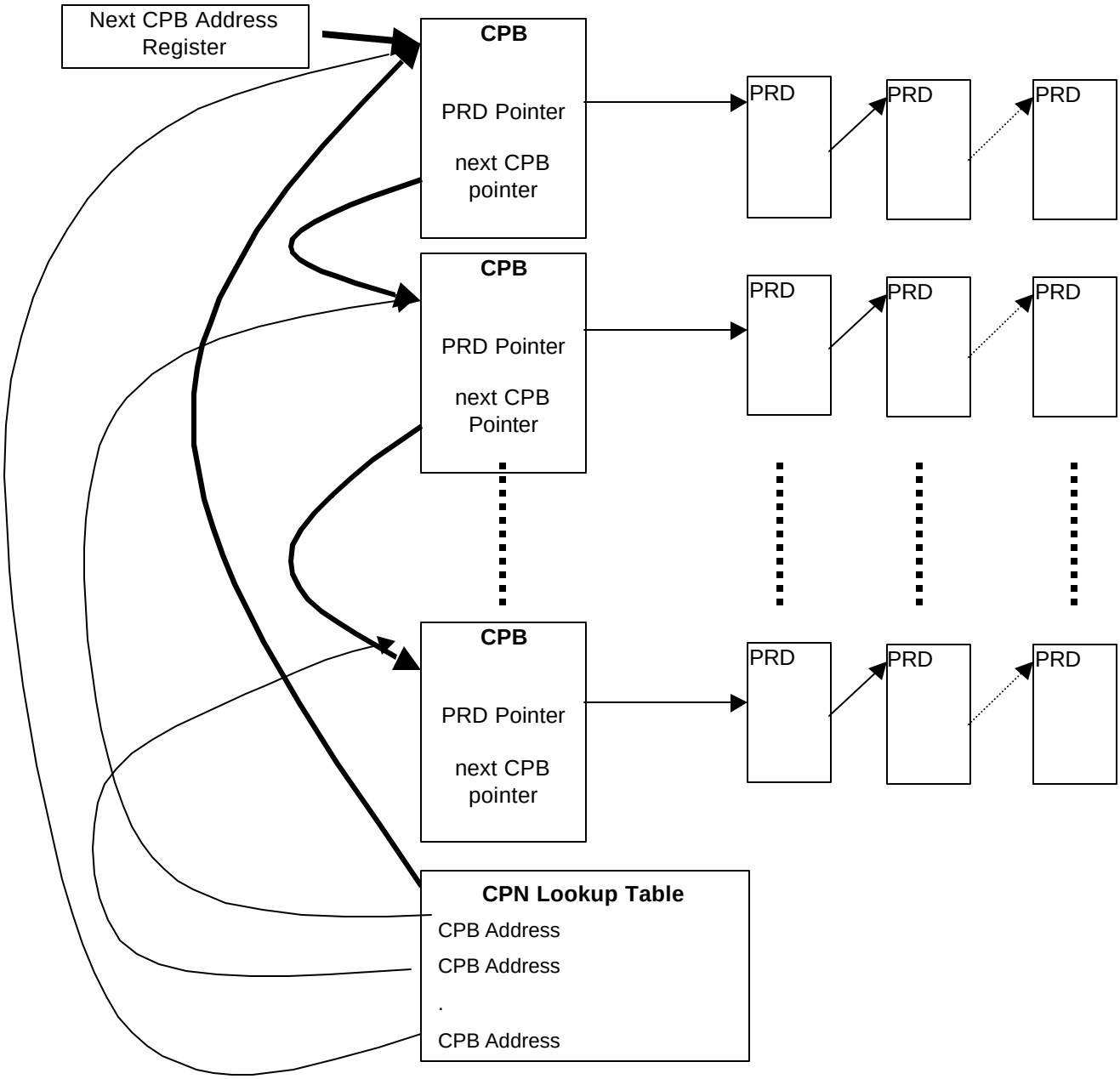

Figure 2. ADMA Memory Usage

6.8.1 Command Parameter Block

The CPB is a block of parameters and commands for the Adapter and, indirectly, for the ATA Channel. All transfers to and from the CPB are 32 bits wide. Any unused space is zero-filled. CPB entries shall all be physically contiguous, locked in memory, and Qword-aligned in physical address space

6.8.1.1 CPB Layout

Quad Word		Byte	Bits	Name	Cntrl	Init	Description
0	Response Flags	0	0	cDONE	P/H	1	The Adapter sets bit 0 to 1 when it has completed processing the command in this CPB entry or cIGNOR is set to one.
			1	cREL	P/H	0	The Adapter sets bit 1 to 1 if it receives an interrupt from the ATA Device with the REL bit set.
			2	cIGNRD	P/H	0	Bit 2 is set to 1 by the Adapter if, on the first access of the CPB entry, cVLD, cREL and cDONE are found to be zero.
			3	cATERR	P/H	0	Bit 3 is set to 1 by the Adapter if the ERR bit in the ATA Device Status register is set to 1 during execution of the command.
			4	cSPNT	P/H	0	The Adapter sets bit 4 to 1 if it detects an unexpected interrupt (spurious interrupt) during execution of a command.
			5	cPSDEF	P/H	0	The Adapter sets bit 5 to 1 if the PRD transfer lengths are insufficient to complete the command.
			6	cPSEXC	P/H	0	The Adapter sets bit 6 to 1 if the PRD transfer length is in excess of that required to complete the command.
			7	cCPBERR	P/H	0	The Adapter sets bit 7 to 1 if it determines that the CPB is inconsistent.
		1	7:0		H		Reserved. Shall be cleared to 0.
	Control Flags	2	0	cVLD	H/P	0	Set to one by the Host to indicate that the CPB is to be processed. If cVLD is set to one and cDONE is cleared to zero, the Adapter shall process the CPB. If cVLD is cleared to zero and cDONE is cleared to zero, the Adapter shall set cDONE and cIGNRD to one and not process the CPB.
			1	cQUE	H/P	0	Bit 1 shall be cleared to zero for non-queued or overlapped commands. Set to Set to one for queued/overlapped commands.
			2	cDAT	H/P	0	Bit 2 is set to 1 to indicate that the PRD contains valid information and the PRD address shall be valid
			3	cIEN	H/P	0	Bit 3 is cleared to 0 to disable the command complete interrupt; set to 1 to allow the Command Complete interrupt.
			4	cIO32	H/P	0	Reserved to indicate transfer to a 32-bit I/O device in a 64-bit environment, in future versions of the Adapter. Shall be set to 0.
			5	cFLIP	H/P	0	Bit 5 is set to one to indicate that DEV shall be toggled at the successful completion of this CPB's ATA command.
			6-7		H/P		Reserved. Shall be cleared to zero.
	CPB Length	3	7:0	cLEN	H/P	0	The length in Qwords of the ATA Command Data Area of the CPB (CPB length = 1 + cLEN Qwords).
	CPB	4-7	31:0	cNCPB	H/P	Next	Memory Address of the next CPB. Shall be Qword aligned.
1	PRD	0-3	31:0	cPRD	H/P		Memory Address of the first PRB. Shall be Qword aligned.
		4-7					Reserved shall be cleared to zero.
2	CMD	0-1	15:0	ATADA0	H/A	0's	ATA Command Data - See description
	CMD	2-3	31:16	ATADA1	H/A	0's	ATA Command Data - See description
	CMD	4-5	47:32	ATADA2	H/A	0's	ATA Command Data - See description
	CMD	6-7	63:48	ATADA3	H/A	0's	ATA Command Data - See description
⋮	CMD	⋮	⋮	⋮			⋮
n	CMD	0-1	15:0	ATADAn-3	H/A	0's	ATA Command Data - See description
	CMD	2-3	31:16	ATADAn-2	H/A	0's	ATA Command Data - See description
	CMD	4-5	47:32	ATADAn-1	H/A	0's	ATA Command Data - See description
	CMD	6-7	63:48	ATADAn	H/A	0's	ATA Command Data - See description

Table 13 – CPB Structure

The Host writes the CPB data and except the Response Byte the Adapter does not change the data.

6.8.1.2 Response Flags (Byte 0)

The Adapter writes these flags during the processing of the CPB. They shall be set to zero by the Host when preparing the CPB. They are in a byte by themselves, so that the Adapter does not have to do a read/modify/write operation.

If the CPB chain is to be modified (i.e., the NCPB pointer), the Host shall first PAUSE the Adapter to prevent it from following an invalid chain.

6.8.1.2.1 cDONE – ATA Command Complete Flag (Bit 0)

The Adapter sets this flag to 1 when it has completed processing the command in this CPB entry. It is used by the Adapter to prevent processing the CPB again on subsequent passes round the CPB chain. If this bit is set to one, the Host has control of the CPB.

The Host clears cDONE to zero and sets cVLD to one to indicate that the CPB contains valid command information. Thereafter the only action allowed by the Host is clearing cVLD to zero as an attempt to abort the CPB.

6.8.1.2.2 CREL ATA Release Interrupt Flag (Bit 1)

The Adapter sets this flag to 1 when it receives an ATA interrupt with the REL bit set in the ATA Sector Count Register during a queued command (cQUE flag set). When the Adapter has set this flag, it can proceed to find the next valid CPB to execute.

6.8.1.2.3 cIGNRD – CPB Ignored (Bit 2)

If the Adapter reads a CPB with both cDONE and cVLD cleared to zero, it sets both cDONE and cIGNRD to one, sets aDONE, and asserts pINTA. The CPB is ignored and the next CPB in the chain is processed. If the CPB is being accessed due to a Service Interrupt, cVLD is assumed to be set to one.

6.8.1.2.4 cATERR – ATA Command Error Flag (Bit 3)

This flag is set to 1 by the Adapter if it detects that the ERR (CHK) bit set in the ATA Status (or Alt Status) Register during the command. When the Adapter sets this bit, it sets aCPBERR, asserts pINTA and stops. The Host is responsible for error recovery.

6.8.1.2.5 cSPNT – ATA Spurious Interrupt Error Flag (Bit 4)

The Adapter sets this flag to 1 if the INTRQ is asserted unexpectedly during execution of a command. When the Adapter sets this bit, it sets aCPBERR, asserts pINTA and stops. The Host is responsible for error recovery.

6.8.1.2.6 cPSDEF – PRD Deficient Length Error Flag (Bit 5)

The Adapter sets this flag to 1 if the total transfer length in the PRD chain is insufficient to complete the ATA transfer. In this situation, the ATA Device may be hung, or data may have been lost. When the Adapter sets this bit, it sets aCPBERR, asserts pINTA and stops. The Host is responsible for error recovery.

6.8.1.2.7 cPSEXC – PRD Excess Length Error Flag (Bit 6)

The Adapter sets this flag to 1 if the transfer is complete before the PRD length expires. In this case, the Device shall have completed the command, with or without errors. When the Adapter sets this bit, it sets aCPBERR, asserts pINTA and stops. The Host is responsible for error recovery.

6.8.1.2.8 cCPBERR – ATA Command Error Flag (Bit 7)

The Adapter sets this flag to 1 if it detects an inconsistency in the CPB. When the Adapter sets this bit, it sets aCPBERR, asserts pINTA and stops. The Host is responsible for error recovery.

6.8.1.3 Control Flags (Byte 2)

These flags control the detailed operation of the Adapter. They remove the need for the Adapter to recognize the ATA command set. Thus, if new commands are defined, the Adapter can still function.

6.8.1.3.1 cVLD – CPB Valid (Bit 0)

The Host shall set cVLD to one to indicate that the CPB shall be processed when cDONE is cleared to zero. If the Host determines that a CPB need no longer be processed, it may clear cVLD to zero. The Host shall not set cDONE to one. If the Adapter accesses the CPB after this bit is set, the Adapter shall ignore the CPB and indicate such, using cIGNRD. If the CPB is released, the Adapter shall ignore the state of this bit when accessing the CPB in response to an ATA SERVICE interrupt.

6.8.1.3.2 cQUE – Overlap/Queue Flag (Bit 1)

This bit is set to one to indicate that the command set contains an overlapped or queued command. This bit cleared to zero indicates that there is no queued or overlapped command. If this flag is set, the Adapter inspects the SERV Bit in the ATA Status Register and the REL Bit in the ATA Sector Count Register, on the assertion of ATA INTRQ.

6.8.1.3.3 cDAT – PRD Valid Flag (Bit 2)

The Host shall set this flag to 1 to indicate that CPRD (Dword 2) is valid. The PRD chain may contain Directed Interrupt Information, Packet data pointers, or data transfer pointers, or any combination of these.

6.8.1.3.4 cIEN – PCI Interrupt Enable Flag (Bit 3)

The Host shall clear this flag to 0 to prevent the Adapter from generating a PCI INTA when the command is complete. It shall set this flag to 1 to allow the PCI INTA. Clearing this flag shall not prevent a PCI pINTA if the Adapter stops because of an error.

6.8.1.3.5 CIO32 – Thirty-Two Bit I/O Flag (Bit 4)

This flag is reserved for future use. It is intended to signal I/O transfers to a 32-bit Device in a 64-bit environment. The Host shall clear this flag to 0 for the current hardware.

6.8.1.3.6 cFLIP – Flip DEV Flag (Bit 5)

If this flag is set to one, the Adapter shall invert the current value of DEV when the last ATA command has completed successfully. The END bit in the CPB ATA command structure indicates the last ATA command. If ATA ERR is set, the DEV bit is not inverted.

6.8.2 cLEN-CPB Length (Byte 3)

This Byte contains the number of Qwords that follow Dword2. This enables the Adapter to correctly request the number of Dwords to fetch for any particular CPB.

6.8.3 NCPB - Next CPB Address (Dword 1)

The Host, at initialization, shall construct in memory a circular chain of CPBs, each of which is physically contiguous and Qword-aligned in physical address space. Each CPB shall have in this field the physical address of the next CPB. The Host shall write the address of the first CPB into the ADMA Next CPB Address Register before setting the aGO bit in the ADMA Control Register.

If the Host needs to change the chain pointers while the Adapter is running, it shall first PAUSE the Adapter by setting the aPSE bit in the ADMA Control Register and checking that the aPSD bit in the ADMA Status Register has set. This prevents the Adapter from using any of the pointers.

6.8.4 cPRD – PRD Address (Dword 2)

The Host, at initialization, shall construct PRD control, as required, so that each CPB has a corresponding PRD chain with the first PRD physical address in this field.

6.8.5 ATADAn ATA Command Data Entry

The ATA Command Data is a list of 16-bit fields describing the ATA register writes involved in the command sequence. Each Qword CPB entry contains four 16-bit fields.

Bits 7:0, 23:16,39:32, 55:48 contains the bit pattern to be written to the register.

Bits 12:8 ,28:24, 44:40, 60:56 are used to indicate the ATA command or control register to address. The bits directly map onto the register address to be mapped.

Bit 13 , 29, 45, 61 (IGN)shall be set to one to cause the Adapter to ignore the 16 bit word. This may be used to pad the last ATA Command Data Entry to ensure that the last valid field is the last 16 bit word of the entry, Bit 14, 30, 46, 62 (WNB) shall be set to 1 to cause the Adapter to wait for the ATA Device to go Not Busy (BSY = 0) before writing the data. It shall be cleared to 0, otherwise.

Bit 63 (END) shall be set to 1 in the last 16-bit field and shall be cleared to 0, otherwise. Note that the last field shall be the last word of a Quad word ATA Command Data Entry.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	WNB	IGN	CS1	CS0	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	WNB	IGN	CS1	CS0	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
0	WNB	IGN	CS1	CS0	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
END	WNB	IGN	CS1	CS0	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Table 14 – ATA Command Data

The Adapter scans in the CPB, reading the ATA Command data double words into its FIFO. When the Adapter detects the END bit set, it stops scanning.

6.9 PRD Chain

Each PRD Chain contains a variable number of entries (PRDs). The PRD chain shall be locked in memory and Qword-aligned in physical address space. The information in the PRD chain is derived by the Host from the operating system's memory manager, and describes the physical addresses corresponding to the logical buffer address in the original I/O request. There can be several PRDs to describe a transfer buffer because some processors fragment physical memory by the use of paging registers.

In the case of an ATAPI Packet Command, the first PRD is used to describe the packet itself.

In the case of Directed Interrupts, the PRD contains the target Memory or I/O address and the Data to be written to the address.

6.9.1 Physical Region Descriptor

Each Physical Region Descriptor (PRD) is 2 Qwords in size and describes a contiguous region of memory involved in the transfer or an I/O address. The controller reads each PRD, in turn, and transfers data to or from the PRD-associated memory block or I/O address, until the ATA Device interrupts to indicate the end of the transfer. If the transfer length described by the current PRD is exhausted, the controller reads the next PRD and continues.

If the last PRD space is exhausted and the ATA Device has not interrupted, the Adapter halts execution, after first setting cPSDEF and aCPBERR to one and then asserting pINTA.

If the Device has completed the command and the last PRD space is not exhausted, the Adapter halts execution, after first setting cPSEXC and aCPBERR to one and then asserting pINTA.

Qword	Byte	Bits	Name	Description
0	3:0	31:0	pMAD	Physical address of the start of a physically contiguous memory region. Shall be Qword-aligned. If an I/O transfer, the I/O address of the source or destination of the data.
	7:4	31:0	pLEN	Length, in Qwords, of the transfer segment.
1	0	0	Reserved	
		1	pIGEX	Ignore Data Excess. Set to one to indicate to the Adapter that data excess occurring in this PRD is not an error. This is primarily used when reading the results from certain ATAPI packet commands that return unknown or odd lengths of data. cPSEXC shall be set but no interrupt will be generated.
		2	pPKT	Set to one to indicate that pMAD is a pointer to a Packet (pLEN indicates the total length of the data transfer). pDINT shall be cleared to zero.
		3	pDINT	Set to one to indicate that a Directed Interrupt (DINT) is to be performed, if a non-error interrupt event occurs. pMAD is the memory or I/O address to which to write the message. pLEN contains the 'message', which should be the physical address of the first Dword of the associated CPB and pIOM indicates I/O or memory operation. Note that pINTA is controlled by cIEN only (both Directed Interrupts and pINTA may be enabled, depending on the respective states of pDINT and cIEN).
		4	pORD	Data Transfer method. Shall be set to 1 for UltraDMA, cleared to 0 for DMA-assisted PIO.
		5	pDIRO	Data Transfer Direction. Shall be set to 1 for output to the ATA Device, cleared to 0 for input from the ATA Device.
		6	pIOM	Set to one for I/O transfers, cleared to zero for Memory transfer.
		7	pEND	In the last PRD entry of a PRD chain, pEND shall be set to one and pNXT shall be cleared to zero.
	1	0:3	pTMOD	PIO Mode or Ultra DMA Mode to use, depending on pORD (Bit 4)
		4:6	pCRC	If pORD is set to 1, this field shall define the burst size that the Adapter shall use before terminating and sending a CRC. A value of 000b shall indicate that the entire block is transferred. Values 001b to 111b indicate the burst size in 512-Byte units.
		7	pPKLW	Packet length in words if pPKT is set to one.
	3:2	0:7		Reserved. Shall be cleared to zero.
	7:4	31:0	pNXT	Physical Address of the Next PRD. In the last PRD entry of a PRD chain, pNXT shall be cleared to zero and pEND shall be set to one.

Table 15 – Physical Region Descriptor (PRD).

6.10 CPB LookUp Table

The Host shall construct a CPB Look-Up Table (and write its physical address to the ADMA Look-Up Table Address Register prior to starting the Adapter) if overlapped or queued operation is to be allowed. The table shall be physically contiguous, locked in memory and Qword-aligned in physical address space. Each entry shall be a Dword and contain the physical address of the CPB that is defined by the address calculation below. Note that, if the CPB chain is modified by the Host (while the Adapter is PAUSED), this table shall be updated before restarting the Adapter.

The CPB Look-Up Table is used to restore the original CPB in the case of overlapped or queued operation. In these cases, when an ATA interrupt is received with the SERV bit set, the Adapter retrieves the ATA Tag field from the Device and uses it to construct an address within this table. If sub-channels are in use (SCEN set to 1), the Adapter also retrieves the current sub-channel from the channel by means of a Channel Command. The address calculation is:

CPB Lookup Table Address Register + (SUB * 200h) + (DEV * 100h) + (TAG * 08h)

(If aSUBEN is cleared to 0, SUB is defined to be 0)

6.11 Operation

6.11.1 Operating Modes

The Adapter is either in Legacy or ADMA Mode. When in Legacy Mode, the ATA legacy registers are directly accessible from the Host and any ATA INTRQ assertion causes an assertion of pINTA. In ADMA Mode, the ATA registers are not accessible by the Host.

6.11.2 Interrupt Assertion (pINTA)

The Adapter shall assert pINTA whenever it sets one or more of the following bits: aDONE, aPSD, aUIRQ, aCPBERR and aPERR in ADMSTAT. The only exception to this is the setting of aDONE. Setting aDONE to one shall normally cause the assertion of pINTA unless cIEN in the current CPB is cleared to zero. The Adapter shall assert pINTA whenever an ATA INTRQ interrupt line is asserted during Legacy Mode.

6.11.3 Host Reading ADMA Status Register (ADMSTAT)

After the Host has read the ADMSTAT register, normally in response to an interrupt, the Adapter shall clear aDONE to zero and negate pINTA.

6.11.4 Adapter response to Host clearing aGO

When the Host writes a zero to aGO, and the Adapter is currently idled, the Adapter shall clear aCPBERR and aPERR to zero. This assures the Adapter stays in an idle state, during an error condition, until the Host finishes its error handling and reissue a one to aGO. The Adapter would not response to aGO being cleared while it is not idled or paused.

6.11.5 ADMA Operational Modes State Diagram

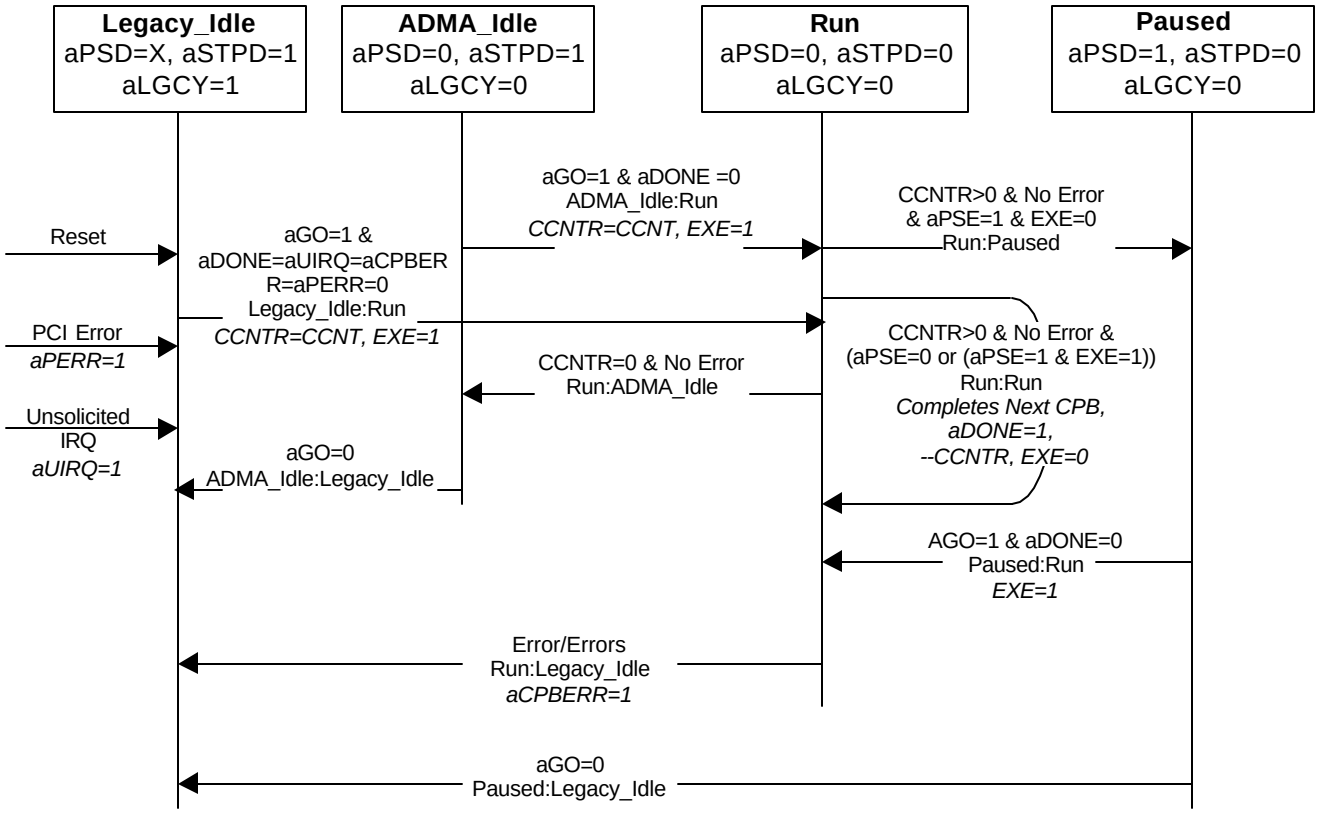

Figure 3. ADMA Operational Modes State Diagram

State diagram convention shall be as described in ATA/ATAPI-5, revision 1C, and Section 3.2.7.

The Adapter can be in one of four states: Legacy_Idle, ADMA_Idle, Run, or Paused. When in the Run, Paused or ADMA_Idle states, the Adapter is in ADMA Mode. When in the Legacy_Idle state, it is in Legacy Mode.

There are two CPB executing modes: Single-step CPB Execution Mode and Continuous CPB Execution Mode. In Single-step CPB Execution Mode, the Adapter shall complete one valid CPB, interrupt the Host, then wait until the Host reads the ADMSTAT register before continue executing the next CPB. In Continuous CPB Execution Mode, the Adapter shall continuously execute each CPB to completion without stopping unless an error occurs.

The state transitions are controlled by the values in the ADMA Control Register and the current value in CCNTR. The Adapter reports its current operating mode and other status in the ADMA Status Register.

6.11.5.1 Legacy_Idle State:

This state is entered when a power-on, hardware, or software reset has occurred. This state is entered when Host aborts an ADMA operation (Hosts clears aGO), or when an error condition occurs. In this state, all ATA registers are accessible by the Host. In this state, the Adapter shall set aSTPD to one and aLGCY to one.

Transition Legacy_Idle:Run: When a one is written to aGO, and the states of aDONE, aCPBERR, aUIRQ and aPERR are all zeros, the Adapter shall initialize CCNTR with the contents of CCNT, set the EXE flag to one (an indication to Run state to proceed with the execution of the next CPB) and make a transition to Run state.

6.11.5.2 ADMA_Idle State:

In this state, the Adapter shall clear aPSD to zero, sets aSTPD to one, and clears aLGCY to zero. The Adapter shall return 0x80 (ATA Device BSY bit set) in response to Host reading any of the ATA registers. The Adapter shall ignore any writing to the ATA registers.

Transition ADMA_Idle:Run: When a one is written to aGO, and the states of aDONE, aCPBERR, aUIRQ and aPERR are all zeros, the Adapter shall initialize CCNTR with the contents of CCNT, set EXE flag to one (an indication to Run state to proceed with the execution of the next CPB) and make a transition to Run state.

Transition ADMA_Idle:Legacy_Idle: When aGO is cleared to zero, the Adapter shall make a transition to Legacy_Idle.

6.11.5.3 Run State:

In this state, the Adapter shall clear aPSD, aSTPD and aLGCY to zero. All Adapter runtime tasks are carried out in this state. These tasks include fetching a CPB entry, completing the CPB as according to its contents, reporting CPB completion status if required, accessing the CPB Lookup Table in response to an ATA service request, controlling data transfer across the PCI interface to/from the device.

Transition Run:Run: When aPSE is cleared to zero (Host commands Continuous CPB Execution Mode), or aPSE is set to one and EXE is set to one (Host starts Single-step CPB Execution Mode), and CCNTR is not zero and no error has occurred, the Adapter shall search through the CPB chain to find and execute a valid CPB. After a CPB is completed with or without error, it shall update the CPB Response byte (cDONE, cREL, cIGNRD, cATERR, cSPNT, cPSDEF, cPSEXC and cCPBERR), set aDONE to one, assert pINTA, decrement CCNTR counter, clear EXE flag to zero (indicates to Run state that this CPB is completed) and make a transition to Run state.

Transition Run:Paused: When aPSE is set to one, EXE is cleared to zero (a CPB is completed in single-step mode), CCNTR is not zero, and no error has occurred, the Adapter shall make a transition to Paused state.

Transition Run:Legacy_Idle: When an error occurs, the Adapter shall set the appropriate error bit in the CPB Response byte, set aCPBERR to one, assert pINTA and make a transition to Legacy_Idle state.

Transition Run:ADMA_Idle: When CCNTR is zero, and no error has occurred, the Adapter shall make a transition to ADMA_Idle state.

6.11.5.4 Paused State:

This state is entered after a CPB has successfully completed during a Single-step CPB Execution Mode.

In this state the Adapter shall set aPSD to one and clear aSTPD and aLGCY to zero.

Transition Paused:Run: When aDONE is cleared to zero as a result of Host reading the ADMA Status Register (ADMSTAT), the Adapter shall set EXE flag to one (indicates to Run state to continue executing the next CPB) and make a transition to Run state.

6.11.6 Error Handling

The Adapter can detect the following types of error condition: ATA Error, ATA Spurious Interrupt, CPB Error, PRD's data transfer length and actual data transfer length discrepancies, and PCI Error. Each of these errors except PCI Error are reported in the CPB Response Byte, aCPBERR shall be set to indicate that errors are being reported in the CPB Response Byte. A PCI Error is reported in ADMSTAT. In all instances of an error occurring, the Adapter shall transition to the Legacy_Idle state and ignore a write of one to aGO until ADMSTAT is read.

6.11.6.1 ATA Error (cATERR)

The Adapter has detected that the ATA Status register has ERR set to one. In ATA Devices, this indicates that some kind of error has occurred. In ATAPI Devices, this may indicate an error or a check condition. Upon

detecting ERR set to one, the Adapter shall set cATERR to one, set aCPBERR to one, assert pINTA and transition to Legacy_Idlestate.

In this case, the Host software shall assume that the CPB did not complete successfully and data may or may not have been transferred with or without errors.

6.11.6.2 ATA Spurious Interrupt (cSPNT)

The Adapter detected an ATA INTRQ assertion, when not expected, while in the Run state. The Adapter shall set cSPNT to one, set aCPBERR to one, assert pINTA and transition to the Legacy_Idle state.

A spurious interrupt can indicate a faulty ATA channel with a Device malfunctioning. The Adapter can only assume that any further processing of a CPB will have undetermined results. Consequently, any data transfers in progress to the Device shall be stopped, data transfers from the Device shall be discarded (the CPB is aborted). The Adapter does not try to terminate an ULTRA DMA burst or transfer a CRC to the Device, as the Device's ability to process the sequence is in question.

If an ULTRA DMA read from the Device is in progress and the Device does not stop sending data when ATA STOP is asserted, accesses by the Host to ATA registers shall follow the ADMA mode rules (see**6.7.1**). In such circumstances, the Host may attempt to regain control of the ATA channel by toggling aRSTA in ADMCTL.

6.11.6.3 CPB Inconsistency Error (cCPBERR)

This error will occur if an ATA service interrupt points to a CPB that has not been released. In this case, the Adapter shall set cCPBERR and aCPBERR to one, assert pINTA and make a transition to Legacy_Idle state.

6.11.6.4 PCI Error (aPERR)

If the Adapter detects a PCI error, it is an indication of a severe system problem. Any transfers across the PCI bus are now suspect and may result in catastrophic failure. The Adapter shall cease all ATA operations, set aPERR to one, assert pINTA, and transition to Legacy_Idle state. The Adapter does not attempt to update the CPB, as this would involve a complete master mode operation on the suspect PCI bus. The Host software shall take whatever actions it can to determine the state of the bus, before attempting any more accesses to the Adapter.

The bit aPERR will be set whenever bits 8, 12, 13 or 15 of the PCI status register are set to one. If the PCI command register bit 6 is set (parity error response enabled), the PCI core will issue assert pPERRn. Otherwise, the PCI core inside the Adapter shall set bit 15 in the ADMA Status register and continue on as if nothing happened

The PCI aPERR bit will be cleared by a read of the ADMA status register. The interrupt signal pINTA will remain asserted until pPERRn is cleared to zero.

6.11.7 CPB Initialization

The Host shall ensure that there is a correctly initialized CPB chain before starting the Adapter. A valid CPB chain shall consist of one or more CPB structures with the Next CPB fields pointing to the physical memory address of the next CPB in the chain (the Next CPB field in a chain of one CPB would point to itself). cDONE shall be set to one and cREL shall be cleared to zero in each CPB. A Valid CPB Lookup table shall be constructed. The Host shall write the address of the first CPB into the Adapter Next CPB Address register and the start of the contiguous CPB Lookup table into the ADMA Lookup Table Address register.

Before updating the CPB chain pointer, the Host shall ensure that the Adapter has STOPPED or PAUSED, by examining aSTPD and aPSD.

6.11.8 Adapter Initialization

The Host shall ensure that there is a correctly initialized CPB chain before starting the Adapter. A valid CPB chain shall consist of one or more CPB structures with the Next CPB fields pointing to the physical memory address of the next CPB in the chain (the Next CPB field in a chain of one CPB would point to itself). Bit cDONE shall be set to one, cVLD and cREL shall be cleared to zero in each CPB. A Valid CPB Lookup table shall be constructed. The Host shall write the address of the first CPB into the ADMA Next CPB Address register (NCPB) and the start of the contiguous CPB Lookup table into the ADMA Lookup Table Address register (LTAR).

6.11.9 Non-Queued Operation

The Host software assembles a CPB entry in the Host’s memory and sets the GO bit in the ADMA Control Register to initiate a data transfer. Starting from the current value in the ADMA CPB Address Register, the Adapter reads the current CPB using a PCI master mode burst.

During the CPB read:

- the contents of the CPB ATA command block are transferred into the Adapter FIFO,

- the Next CPB Address register is updated from the CPB to point to the next CPB in the chain,

- the PRD Address register is updated to point to the start of the PRD chain,

- the CPB Control register is updated.

If the CPB is valid, the CPB Command Interpreter interprets it. The ATA Device registers are written to initiate the transfer, and the internal ADMA registers are initialized using data from the current CPB entry. If the CPB is not valid, the next CPB is read until a valid entry is found or the CPB count register has decremented to zero.

If the ATA data transfer is via PIO, the Adapter monitors the ATA Status Register and the ATA INTRQ signal, to determine when the Device is ready to transfer data.

If the transfer is via Ultra DMA, the ATA Device indicates that it is ready, by asserting ATA DMARQ.

If the CPB involves a data transfer, the PRD Address Register is used to load the first PRD entry, using a PCI master mode burst. The data address within this entry is loaded into the PCI Master Mode Address register, the count into the PCI Master Mode Count register, the next PRD address into the ADMA Next PRD register and the control information into the ADMA transfer Control register. During the data transfer, the PCI Master Mode Address Register is incremented and the Count is decremented, on each Dword transferred from or to the FIFO across the PCI bus. By maintaining the current memory location in the registers, the Adapter is able to start a new PCI burst, if either the Adapter or the PCI Host removes the current burst grant before the count expires to zero.

When the PRD count decrements to zero, the Adapter accesses the next PRD entry, using the ADMA Next PRD register, unless the current one indicates that it is the last.

At the conclusion of a CPB, the Adapter shall update the CPB with status information. The PCI INTA shall then be asserted if the Host interrupt bit is set in the CPB or if an ATA error occurs.

6.11.10 Queued Operation

If the Device Driver and the ATA Devices support Command Overlap and Queuing, the sequence becomes more complicated. The exact protocol differs for ATA and ATAPI Devices. Only certain commands may be overlapped or queued. On each such command, a bit in the CPB indicates it can be queued. After writing the command to the ATA Device, the Adapter waits for an INTRQ or DMARQ to be asserted.

If the Device is ready to transfer data, it may either assert DMARQ (DMA transfer in ATA or ATAPI) or assert INTRQ with DRQ set to one (ATAPI only). If the Device is not ready to transfer data for the current command, it may release the ATA bus, by asserting INTRQ with the ATA release bit (REL) set to one. In either INTRQ case, the ATA service bit (SERV) may be set to one, to indicate that it is ready to transfer data for a previously queued command.

If INTRQ is asserted and the ATA release bit (REL) is set to one and the service bit (SERV) is cleared to zero, the Adapter sets cREL to one in the current CPB and steps on to the next CPB. If the next CPB is valid, it is executed, writing the command to the specified ATA Device, thereby creating a queue of commands in one or both ATA Devices. If the next CPB is invalid, the Adapter reads CPBs until a valid CPB is found or the internal CPB Count counter has cleared to zero.

If SERV is set to one, the Adapter reads the Device/Head Register to determine the current Device and then writes an ATA Service command to the Device and then polls the ATA status register. If the ATA Data Request bit (DRQ) is set to one, the Adapter reads the tag from the ATA Device and uses it and DEV to construct the address (of the relevant CPB) in the CPB Lookup Table. The Adapter then performs the data transfer as in the non-queued case.

When the ATA bus is in IDLE, the Adapter shall alternately select each Device, every microsecond, to enable a Device to assert INTRQ to indicate that it requires service (auto-poll). Only the selected Device is allowed to assert INTRQ. The Adapter shall stop the auto-poll sequence if INTRQ is asserted or if it is about to access an ATA register. The Adapter shall determine which Device asserted the INTRQ, by reading the ATA Device/Head Register.

If the ATA Device releases the ATA bus, the Adapter shall update the CPB but shall not assert PCI-INTA. At this stage, a CPB is released but not complete.

At the conclusion of a CPB, the Adapter shall update the CPB with status information. The PCI INTA shall then be asserted if the Host interrupt bit is set or if an ATA error occurs.

For channels containing an overlapped Device and a non-overlapped Device, the Auto-Poll enable bit (aAUTEN) cleared to zero. Any CPB for the non-overlapped Device shall have cFLIP set to one. Setting cFLIP to one indicates to the Adapter that it shall toggle DEV at the successful (non-error) completion of the command for the non-overlapped Device, thereby selecting the overlapped Device that may have a current queue.

6.11.11 Channel Commands and Sub-Channels

6.11.11.1 Sub-Channel Selection

Sub-channels are selected by a sub-channel command sent using the ATA command register bank. These commands shall precede any device-specific command in the CPB. If sub-channels are in use, aSUBEN shall be set to one in the ADMA Status register (ASTAT). If sub-channels are enabled, the Host shall include a sub-channel selection command sequence in each CPB.

Although theoretically possible, it is not permitted to have a sub-channel controller and a Device on the same channel. It is permitted to have two sub-channel controllers on the same channel.

It is the responsibility of the Host software to use the sub-channel protocols and commands, to ensure that there is a correct configuration and to establish the channel addresses of channel-command-aware Devices that are on an ATA channel. The sub-channel protocols are described in the {Sub-Channel Spec}.

If sub-channels are enabled, the auto-polling sequence is modified. When the Adapter commences the auto-polling sequence, it issues a “Deselect and Auto-Poll” sub-channel command. This command instructs the sub-channel controller(s) to poll the Devices on their channels but not pass through Device selection requests (writes to the ATA Device/Head Register). The Adapter shall then commence the normal auto-polling sequence. When the assertion of INTRQ has been detected, the Adapter shall stop auto-polling and shall issue a “Return Current Selected Sub-channel” sub-channel command. The sub-channel that asserted INTRQ shall reply with its unique identifier. This value is then loaded into the Adapter’s internal current sub-channel register. The Adapter then reads the ATA Device/Head Register, followed by the TAG. The Adapter then has sufficient information to use the CPB Lookup Table to determine which CPB to load to complete a queued transfer.

6.11.12 Enhanced Data Integrity

ULTRA DMA mode transfers include the use of a CRC. The CRC is calculated over the entire block of data transferred. A CRC was introduced into the ULTRA protocol because of the increased risk of data corruption on the ATA cable. Obviously, any form of error detection is a vast improvement over having none. However, the effectiveness of a CRC reduces as the length of the transfer increases. The Adapter has the ability to break each transfer into smaller units, by terminating the burst after transfer of a Host-specified number of Bytes. The number of Bytes in each burst is defined in the PRD for that block of data.

Appendix A

ADMA Programming Guidelines (Informative)

Device driver writers shall familiarize themselves with this whole document. This section is intended to point out some aspects that might not be immediately obvious when writing code to for Adapters in ADMA mode.

A.1 Asynchronous Operation

ADMA .mode adapters operate Asynchronously from the processor. This means that it may process more than one command in between the host being able to service interrupts or even as it is servicing one. Interrupt processing shall bear this fact in consideration.

The host shall be aware that any updates it may make must be undertaken on memory locations that will not be accessed by the Adapter at the same time.

A.2 Memory Alignment

ADMA mode is designed to use QWAD WORD ALIGNMENT. Any transfer requests that the driver may receive from the O/S shall be aligned to a Qwad word boundary. This may mean that the driver has to copy the data to or from an internal Qwad word aligned buffer before/after the ADMA mode transfer.

A.3 Register Usage

ADMA mode adapters provide a set of I/O mapped registers and a 64 bit mapped Memory mapped register. The I/O mapped registers only provide support for legacy operation and are intended for use by system BIOS during initial boot. The Memory mapped registers provide a shadow of the I/O registers as well as the registers needed to control ADMA mode operation. Writers are encouraged to use the Memory mapped registers as the I/O registers may be made obsolete in future versions of the ADMA mode adapters.

A.4 Legacy and ADMA Modes

ADMA mode adapters default to legacy mode at power up, system reset and upon detecting an error. Legacy mode is meant to mean that the ADMA is acting as an address decoder and ATA bus-timing device only. The host reads and writes the ATA devices registers through the two register banks just as it would on a legacy ISA bus paddle card. When using the I/O mapped registers (not recommended) the register addresses are set by the host and usually will not be the legacy 1FX/3FX values. The ADMA does NOT provide separate interrupts for each channel, and thus host software in legacy mode shall use the PCI shared interrupt architecture. Since legacy is primarily used for error handling it is recommended that the drivers poll the registers and not rely on interrupts.

A.5 CPB Chain Initialization

The Host shall ensure that there is a correctly initialized CPB chain before starting the ADMA. A valid CPB chain shall consist of one or more CPB structures with the Next CPB fields pointing to the physical memory address of the next CPB in the chain (the Next CPB field in a chain of one CPB would point to itself). Bit cDONE shall be set to one, cVLD and cREL shall be cleared to zero in each CPB. A Valid CPB lookup table shall be constructed. The Host shall write the address of the first CPB into the Adapter's Next CPB Address register (NCPB) and the start of the contiguous CPB Lookup table into the ADMA Lookup Table Address register (LTAR).

A.6 CPB Chain Management

When a CPB is ready to be processed the Host shall set cVLD to one and clear cDONE to zero. Once cDONE is cleared to zero the ADMA is in control of the CPB. The host shall not modify any CPB with cDONE still cleared to zero unless the ADMA is either in Legacy Idle state or in ADMA_Idle state; and that the CPB to be modified does not have aDONE cleared to zero and cREL set to one. Note that the only exception is the cVLD bit. The host may attempt to stop a CPB from being processed, at any time, by setting cVLD to one. The host shall then wait to ensure that aDONE and cIGNRD have been set before modifying the CPB. If a CPB is being processed when cVLD is cleared the CPB will continue to be processed by the Adapter.

A.7 Resets

A.7.1 PCI Reset

PCI Reset resets the PCI Core, PCI sequencer, ATA sequencer and ATA RESET.

A.7.2 ADMA Reset (aRSTADM)

Channel Reset resets the ATA and PCI state machines. Asserting aRSTADM sets the state machines to their idle state. Registers and data transfers are in an unknown state. The host shall reset all register values. The devices on the channels should be reset and re initialized.

A.7.3 ATA Channel Reset (aRSTA)

Asserting aRSTA asserts the ATA reset signal, de-asserting aRSTA de-asserts the ATA reset signal. The interval between the two should be at least the minimum specified in the relevant ATA standard. An ATA Channel reset shall always be preceded by an ADMA reset.

A.8 Use of aGO

Writing a one to aGO can be thought of as a “door bell”. The intent is to signal to the Adapter that the Host has changed something in the CPB chain. It does not matter that the value of aGO is already one, it is the act of writing a one into aGO in the Adapter’s command register that provides this indication to the ADMA.

A.9 Determining the Current Status of the ADMA

The Host may determine the status of the ADMA by examining the ADMA status register. Figure 3 shows the expected outputs from the status register dependent on the ADMA’s current state. It should be noted that when the ADMA is in ADMA_Idle state, there might be outstanding released CPBs. The Host should examine the CPB chain to determine if there are any released CPBs before modifying the CPB chain.

A.10 Host Pausing of a CPB Chain

The Host may attempt to pause an active chain, at any time, by setting aPSE to one. The Adapter completes any currently active CPB but does not initiate a search of the CPB chain. Upon completion of the current CPB or if no CPB is being serviced, the ADMA sets aDONE to one, cDONE to one and asserts pINTA. If the Adapter is releasing a CPB it shall set cREL to one and transition to the ADMA_Idle state. The Host may determine which CPB just completed, by reading CCPB. The Host may then modify any of the CPB entries in the chain. Host should take care to ensure that CPBs that are released are not invalidated by any changes to the chain and the subsequent changes to the look up table.

Once the Adapter is in Legacy_Idle state, with aPSE and aGO still set to one, the ADMA will continue executing the next CPB after the host has read the ADMA Status register, since aDONE is cleared as result of the host reading ADMSTAT. The host can force the Adapter to resume continuous CPB executing mode at any time by clearing aPSE bit with aGO set to one.

A.11 Host Stopping or Terminating an Active CPB

The host may revert the Adapter to Legacy mode (Legacy_Idle state) by first pausing the Adapter (A.10). When paused the Host clears aGO.

Note that the Host will not get an interrupt if the ADMA was already in either ADMA_Idle or Paused state when the Host clears aGO.

A.12 ATA Interrupts

ADMA mode adapters rely on the use of the ATA bus signal INTRQ. In ADMA Mode, under no circumstances shall Host software set the nIEN bit to one, thereby disabling INTRQ.

A.13 PCI Interrupts

ADMA mode adapters shall assert pINTA whenever it sets one or more of the following bits: aDONE, aPSD, aUIRQ, aCPBERR and aPERR in ADMSTAT. The only exception to this is the setting of aDONE. Setting aDONE to one shall normally cause the assertion of pINTA unless cIEN in the current CPB is cleared to zero. The ADMA shall assert pINTA whenever an ATA INTRQ interrupt line is asserted during Legacy Mode.

After the Host has read the ADMSTAT register, the Adapter will clear aDONE to zero and negate pINTA.

When the Host writes a zero to aGO, and the Adapter is currently in Legacy_Idle state, the Adapter shall clear aCPBERR and aPERR to zero. This assures the Adapter stays in the Legacy_Idle state, during an error condition, until the Host finishes its error handling and reissue a one to aGO.

This means that the host must clear aGO, after all errors have been handled, and set aGO to one if it wishes to command the Adapter to continue executing the next CPB.

A.14 Error Handling

If the Adapter detects that the ATA ERR bit has been set it shall set the appropriate error bits in the CPB and then the bits in the ADMA status register revert to Idle (legacy) and assert an interrupt.

If the Adapter detects a PCI error, it is an indication of a severe system problem. Any transfers across the PCI bus are now suspect and may result in catastrophic failure. The Adapter shall cease all ATA operations, set aPERR to one, assert pINTA, and transition to IDLE (legacy). The Adapter does not attempt to update the CPB, as this would involve a complete master mode operation on the suspect PCI bus. The Host software shall take whatever actions it can to determine the state of the bus, before attempting any more accesses to the Adapter.

Other errors indicate some kind of CPB inconsistency. Data Deficiency (cPSDEF set to one), Excess (cPSEXC set to one) and CPB error (cCPBERR set to one) usually mean that the CPB and PRD were not correctly set up or there has been some type of data transfer error. In some cases the transfer size is known to be other than an exact multiple of quad-words. In such a case the PRD's pLEN shall be rounded up to the nearest Qword length and pIGEX set to one. In this way the Adapter will not stop on error